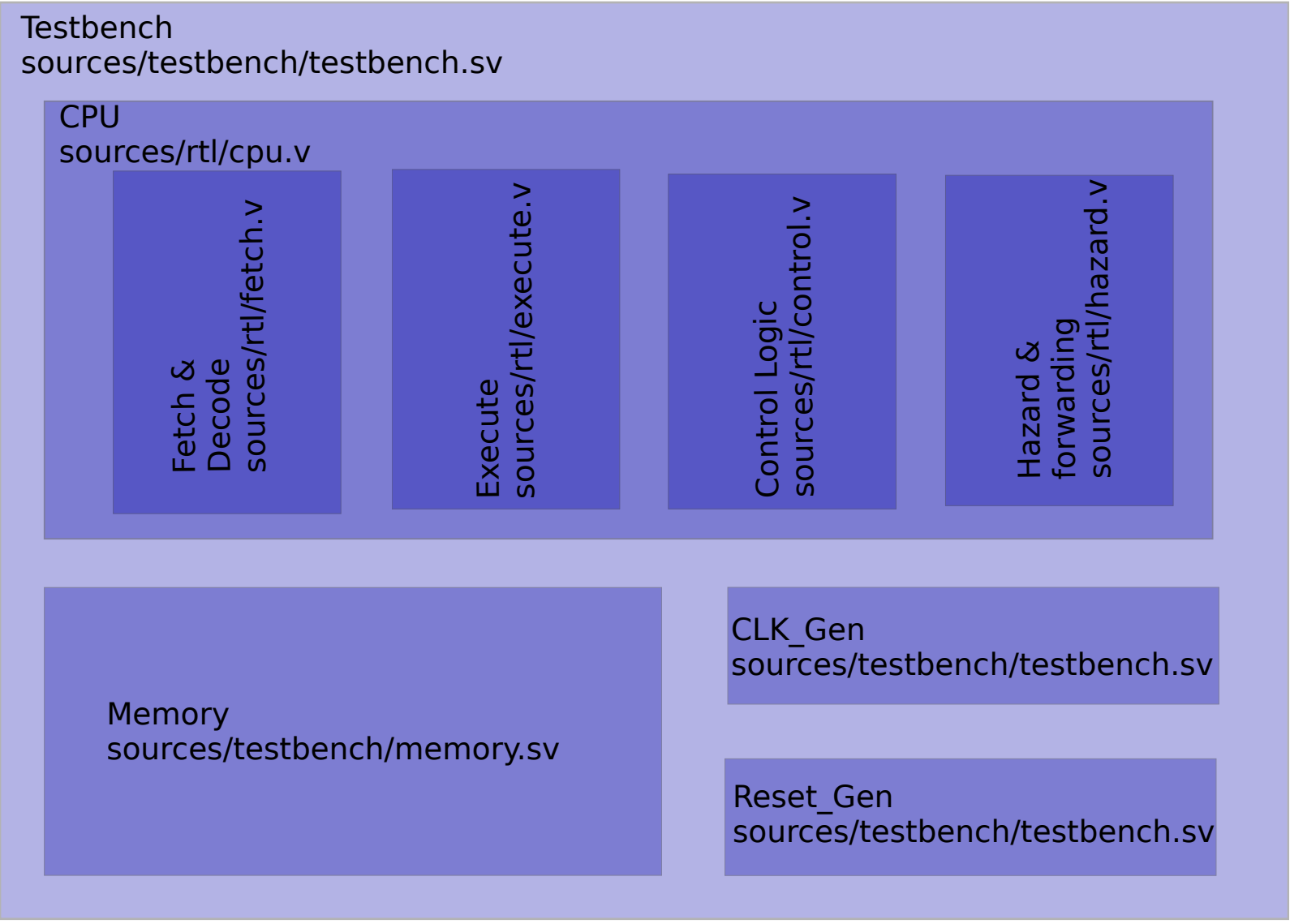
Testbench
sources/testbench/testbench.sv
CPU
sources/rtl/cpu.v
Fetch &
Decode
sources/rtl/fetch.v
Execute
sources/rtl/execute.v
Control Logic
sources/rtl/control.v
Hazard &
forwarding
sources/rtl/hazard.v
Memory
sources/testbench/memory.sv
CLK_Gen
sources/testbench/testbench.sv
Reset_Gen
sources/testbench/testbench.sv